PROCESSOR WITH PROGRAMMABLE ADDRESSING MODES

Abstract of the Invention

A programmable address arithmetic unit and method for use on microprocessors, microcontrollers, and digital signal processors is described. The addressing arithmetic unit incorporates a programmable logic array or other programmable device coupled to address registers and the instruction stream, the address unit being responsive to commands in the processor's instruction set. A first set of instructions control the initialization and configuration of the address arithmetic unit logic. A second set of instructions reference operands using one or more addressing modes that calculate the operand's effective address using the logic programmed by said first set of instructions.

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